performance for a particular application. The device's saturation current level can be adjusted by manipulating the ratio of IGBT structures to bipolar transistor structures, with the saturation current level increased or decreased by increasing or decreasing the ratio, respectively. For example, two BJT structures could be fabricated between each IGBT structure; this would provide a saturation current level lower than would a device having an equal number of the two structures, but would produce a relative increase in forward voltage drop.

The shape of the interdigitated structures is not limited to that of the trench-shaped stripes shown in FIG. **7**. One possible alternative embodiment is shown in the plan view of FIG. **8** (emitter, collector, and gate electrodes not shown for clarity). Here, cylindrical IGBT structures **300** are interdigitated with cylindrical BJT structures **302**. Each IGBT structure is as described above, with a shallow P+ region **304** providing an ohmic contact to the P base region below it (not shown), surrounding by an N+ region **306** and built on a foundation made from an N− drift layer **310** on a P layer **312**. Each BJT structure is also as described above, with a P+ ohmic contact **314** on a P base region (not shown) on the P/N− drift foundation **310**, **312**. Insulated trench gate structures are formed by surrounding each cylindrical IGBT and BJT structure with oxide walls **316**, and horizontal oxide bottoms (not shown) traverse the areas between oxide walls. Shallow P regions (not shown) are preferably employed to protect the oxide corners of the trench gates from peak fields as described above.

Another possible multi-cell embodiment is shown in the plan view of FIG. **9** (emitter, collector, and gate electrodes not shown for clarity) . Here, the continuous stripe trench structures shown in FIG. **7** are broken up into smaller IGBT structures **320** and BJT structures **322**. Each IGBT structure has a shallow P+ region **324** providing an ohmic contact to the P base region below it (not shown), surrounding by an N+ region **326** and built on a foundation made from an N− drift layer **328** on a P layer **330**. Each BJT structure has a P+ ohmic contact **332** on a P base region (not shown) on the P/N− drift foundation **328**, **330**. Insulated trench gate structures are formed by surrounding each IGBT and BJT structure with oxide walls **334**, and horizontal oxide bottoms (not shown) traverse the areas between oxide walls. Shallow P regions (not shown) are preferably employed to protect the oxide corners of the trench gates from peak fields as described above. Breaking up the structures in this way may result in a more uniform turn-on characteristic for the device.

The configurations shown in FIGS. **7**, **8** and **9** are merely exemplary; many other structure shapes (including, for example, squares, squares with rounded corners, and hexagons), and structure ratios (number of IGBT structures/number of BJT structures) could be used to provide a functional device. The trench-shaped stripe structures of FIG. **7** are preferred, as they provide good performance while being easily fabricated. Though not depicted, a multi-cell device could also be implemented with structures of the opposite polarity (per FIG. **4**), with shallow N regions below the trench bottoms to enhance the trench oxide's reliability.

The described devices can be fabricated on punch-through wafers (EPI), in which the drift layer comprises an epitaxial layer grown to a desired thickness and with a proper doping level on a bulk substrate material. The devices can also be fabricated on non-punch-through (NPT) wafers, in which the drift region is a bulk substrate material, and the P layer (such as layer **102** in FIG. **2**) is a thin layer of a material doped with boron which has been implanted or diffused from the backside. Several factors should be considered when determining which wafer-type to use. EPI wafers are more expensive than NPT wafers, but because the epitaxial layer has a controlled thickness and doping concentration, they offer a lower forward voltage drop. An NPT-based device will have a lower hole injection efficiency (if configured per FIGS. **2** or **7**) or a lower electron injection efficiency (if configured per FIG. **4**) than an EPI-based device, and this property can be used to manipulate the stored charge and provide a better switching characteristic. In contrast, lifetime control is used to adjust the stored charge in an EPI-based device. The blocking voltage of the device is affected by the doping level and thickness of the drift layer; a doping level and thickness sufficient to provide a blocking voltage of at least 600 volts is preferred.

The performance of the IGBT is affected by the widths and depths of the trench gates, and by the mesa widths of the IGBT and BJT structures. A trench width of about 2–3 μm, a mesa width of about 3–6 μm, and a trench depth of about 10 μm is preferred, which provides good performance while being practical to fabricate.

While particular embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

I claim:

1. A trench insulated-gate bipolar transistor (IGBT) device with improved safe-operating area (SOA), comprising:

an IGBT structure, comprising:
- a P layer,
- a first electrode which contacts said P layer providing a collector connection for said device,
- an N− drift layer on said P layer opposite said collector,
- a first P base region on said N− drift layer,
- a N+ region on said first P base region, and
- a second electrode which contacts both said first P base region and said N+ region;

a bipolar transistor (BJT) structure adjacent to said IGBT structure, comprising:
- said P layer,
- said N− drift layer,
- a second P base region on said N− drift layer,
- a third electrode which contacts said second P base region, said second and third electrodes connected together and providing an emitter connection for said device; and

an insulated gate arranged in a trench configuration recessed into said N− drift layer between said IGBT structure's N+ and P base regions and said BJT structure's P base region, comprising;
- a layer of oxide in contact with said N+ region, said first P base region, said N− drift layer, and said second P base region, said layer of oxide forming the sidewalls and bottom of said trench gate,
- a conductive material within said trench which connects a voltage applied to the top of said trench to said layer of oxide,
- a shallow P region in said N− drift layer directly adjacent to said trench gate bottom opposite said conductive material which spans the corners formed at the junctions of said sidewalls and said bottom to protect said corners from high peak electric fields when said device is reverse-biased, and
- a fourth electrode which contacts said conductive material providing a gate connection for said device;